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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,576	07/19/2005	Shinichi Hori	Q89211	6882

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EXAMINER	
ROJAS, DANIEL E	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,576	HORI, SHINICHI	
	Examiner	Art Unit	
	DANIEL ROJAS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-20* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/11/2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 5, 7-9, 12, 13, 18, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 19 is objected to because of the following informalities: it is not clearly understood what is meant by “same transistors". For the purposes of examination, “same transistors” will be interpreted as “same size transistors.” Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-10, 12, 13, 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US Patent No. 5,079,443).

6. For claim 1, Wada teaches in his Figure 2 a circuit comprising an active device (Q22) having an input terminal (base), an output terminal (collector), and a grounded terminal (emitter, via Q24 and I20), and carrying out voltage-current conversion (as explained below); and a resistor circuit (R23, R24, Q23, Q24, and I20) electrically connected in series to said active device through said grounded terminal of said active device (as shown), and controlling a conversion gain of said active device (inherent based upon the structure) and including a negative resistance device (Q23, Q24, and I20). Transistor Q22 inputs a voltage (V_B) and outputs a current based on voltage V_B. Therefore, Q22 carries out a voltage to current conversion. It would have been obvious to one of ordinary skill in the art at the time of invention to make constant current source I20 user controllable (i.e. being able to set different constant current values) in order to adjust the voltage level of the output voltage V_O, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

7. For claim 2, the modified version of Wada as defined above further teaches that said active device is comprised of a pair of active devices (Q21, Q22) each operating differentially with each other (as shown), and each having an input terminal (base terminals of each transistor), an output terminal (collector terminals of each transistor), and a grounded terminal (emitter terminal of each transistor), and carrying out voltage-current conversion (as explained below), said resistor circuit is comprised of a pair of resistor circuits (R23 and R24) each electrically connected in series to each of said active devices through said grounded terminal of each of said active devices (as

shown), and each controlling a conversion gain of each of said active devices (inherent based upon the structure), each of said resistor circuits having a variable resistance (as explained below), and including a negative resistance device (Q23 and Q24, respectively). Transistors Q21 and Q22 input a voltage (V_A and V_B, respectively) and output a current based on voltage. Therefore, Q21 and Q22 carry out a voltage to current conversion. As described above, being able to set a user-defined value for the constant current source makes I20 a variable current source (i.e. the value varies based on the user's command). Since the output of the negative resistance devices (Q23 and Q24) are based on the value of the constant current source I20, said resistor circuits have a variable resistance.

8. For claim 3, the modified version of Wada as defined above further teaches said negative resistance device having a variable resistance (as explained below). As described above, being able to set a user-defined value for the constant current source makes I20 a variable current source (i.e. the value varies based on the user's command). Since the output of the negative resistance device (Q23 and Q24) are based on the value of the constant current source I20, said resistor circuits have a variable resistance.

9. For claim 4, the modified version of Wada as defined above further teaches that said resistor circuit is comprised of: one or a plurality of resistance device(s) electrically connected in series to said active device (R22); and said negative resistance device electrically connected in parallel with at said resistance device (as explained below).

Resistor R22 and transistor Q23 are both connected between V_{CC} and ground and are therefore in parallel.

10. For claim 5, the modified version of Wada as defined above further teaches that wherein said resistor circuit is comprised of a first circuit comprised of a resistance device (R24) and a negative resistance device (Q24) electrically connected in series to each other, said first circuit being electrically connected in series to said active device (as shown).

11. For claim 6, the modified version of Wada as defined above further teaches that said resistor circuit is comprised of a first resistance device (R22) electrically connected in series to said active device, and a second circuit electrically connected in parallel with said first resistance device (Q23), said second circuit being comprised of a-said negative resistance device (as explained above), and a second resistance device (R23)electrically connected in series to said negative resistance device. Resistor R22 and transistor Q23 are both connected between V_{CC} and ground and are therefore in parallel.

12. For claim 7, the modified version of Wada as defined above further teaches that said negative resistance device of said pair of resistance circuits is comprised of a pair of active devices (Q23 and Q24) electrically connected in cross to each other and operating differentially with each other (inherent based upon the structure), and each receiving, as an input signal, a node signal either at a connection node at which said active device and said resistor circuit are electrically connected to each other or at any connection node in said resistor circuit (as shown).

13. For claim 8, the modified version of Wada as defined above further teaches that said negative resistance device is comprised of a bipolar transistor (BJTs Q23 and Q24)

14. For claim 9, the modified version of Wada as defined above further teaches that a resistance of said negative resistance device is controlled by controlling either a source voltage or an emitter voltage of said field effect transistor or bipolar transistor (inherent based upon the structure).

15. For claim 10, the modified version of Wada as defined above further teaches a voltage-providing circuit (I20) electrically connected between a reference voltage point (ground) and either a source or an emitter of said field effect transistor or bipolar transistor (as shown), and wherein a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit (via the user, as defined above).

16. For claim 12, the modified version of Wada as defined above further teaches that said negative resistance device is comprised of a pair of bipolar transistors (Q23 and Q24) operating differentially with each other (as shown), wherein sources or emitters of said field effect transistors or bipolar transistors are electrically connected to each other (as shown).

17. For claim 13, the modified version of Wada as defined above further teaches a voltage-controller (I20) electrically connected to a connection node at which said active device and said resistor circuit are electrically connected to each other (emitter of Q22), for controlling a voltage of said connection node (inherent based upon the structure).

18. For claim 15, the modified version of Wada as defined above further teaches that said voltage-controller is capable for compensating for voltage fluctuation caused at said connection node by variance of a resistance of said negative resistance device (based upon the user's commands).

19. For claim 16, the modified version of Wada as defined above further teaches that said resistor circuit includes a variable resistor (I20) having a positive resistance (inherent based upon the structure).

20. For claim 18, the modified version of Wada as defined above further teaches that said active device is comprised of a field effect transistor or a bipolar transistor (Q22).

21.

22. Claims 14 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang.

23. For claim 14, the modified version of Wada as defined above teaches the user-controllability of the current source I20. However, Wada is silent to the details of how to implement user defined control of a current source. Examiner takes official notice that it is notoriously old and well known that variable current sources can be implemented as transistors controlled via a bias signal at the control terminal (i.e. gate or base terminal). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a transistor with a user-controlled bias signal at the control terminal of the said transistor as Wada's current source I20 since all of the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change to their respective functions, and the

combination would have yielded predictable results to one of ordinary skill in the art at the time of invention.

24. For claim 17, the modified version of Wada as defined above further teaches that said variable resistor is comprised of an active device (a transistor, as noted in the rejection of claim 14).

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada.

26. For claim 19, the modified version of Wada as defined above teaches the circuit of claim 1 but fails to teach the limitations of claim 19. Examiner takes official notice that p-type transistors can be substituted for n-type transistors and vice versa. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention that Wada's active device and negative resistance device can be implemented as transistors of electrical conductivities different from each other since the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of invention. Furthermore, Wada's disclosure is silent to the size of the said transistors. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to have transistors Q22, Q23, and Q24 be identically sized since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

27. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada.

28. For claim 20, Wada teaches in his Figure 2 a circuit including a combination circuit comprised of a voltage-current converting circuit, , wherein a pass band is

controlled by varying a gain of said voltage-current converting circuit (inherent based upon the structure), said voltage-current converting circuit comprising: an active device (Q22) having an input terminal (base), an output terminal (collector), and a grounded terminal (emitter), and carrying out voltage-current conversion (as explained below); and a resistor circuit (R23, R24, Q23, Q24, I20) electrically connected in series to said active device through said grounded terminal of said active device, controlling a conversion gain of said active device (inherent based upon the structure), said resistor circuit comprising a negative resistance device (Q23 and Q24) but fails to teach that said resistor circuit having a variable resistance and a capacity device. However, examiner takes official notice that it is notoriously old and well known in the art to connect the output of a circuit to ground via a capacitor in order to filter noise and ground jitter. Therefore, it would have been obvious to one of ordinary skill in the art to connect a capacitor from the output node (Vo) to ground in order to filter noise and ground jitter. Said capacitor is a capacity device. Furthermore, transistor Q22 inputs a voltage (V_B) and outputs a current based on voltage V_B. Therefore, Q22 carries out a voltage to current conversion. It would have been obvious to one of ordinary skill in the art at the time of invention to make constant current source I20 user controllable (i.e. being able to set different constant current values) in order to adjust the voltage level of the output voltage V_O, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Allowable Subject Matter

29. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816
7/29/2008